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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/804,054 | 03/19/2004 | Masashi Shima | 042257 | 7067 |

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| EXAMINER | |
|---|---|
| QUINTO, KEVIN V | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/804,054 | SHIMA, MASASHI | |
| | Examiner | Art Unit | |
| | Kevin Quinto | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,6,9,12,13 and 18* is/are rejected.

7)☒ Claim(s) *2-4,7,8,10,11 and 14-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *19 March 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Specification*

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Puchner et al. (USPN 6,544,854 B1).

4. In reference to claim 1, Puchner et al. (USPN 6,544,854 B1, hereinafter referred to as the "Puchner" reference) discloses a similar device. Figure 7 of Puchner discloses a semiconductor device with a channel layer of SiGe (20) formed over a silicon substrate (12). The SiGe channel layer is formed at a thickness of 30 angstroms or 3 nm (column 4, lines 13-18). A gate electrode (24) is formed over the channel layer (20) with a gate insulation film (22) formed between them. A source (40) and a drain (40) are formed on both sides of the gate electrode (24).

5. In reference to claim 13, Puchner (USPN 6,544,854 B1) discloses a similar device. Figures 1-7 of Puchner disclose a method of fabrication for a semiconductor device with a channel layer of SiGe (20) formed over a silicon substrate (12). The SiGe channel layer is formed at a thickness of 30 angstroms or 3 nm (column 4, lines 13-18). A gate electrode (24) is formed over the channel layer (20) with a gate insulation film (22) formed between them. Figure 5 shows an implantation of a dopant impurity into the silicon substrate (12) using the gate electrode (24) as a mask to form first impurity diffused regions on both sides of the gate electrode (24). A sidewall insulation film (34 or 36) is formed on the sidewall of the gate electrode (24). Figure 6 shows an implantation of a dopant impurity into the silicon substrate (12) using the gate electrode (24) and the sidewall insulation film (34 or 36) as a mask to form second impurity diffused regions on both sides of the gate electrode (24).

6. Claims 1 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Yagishita et al. (USPN 6,815,279 B2).

7. In reference to claim 1, Yagishita et al. (USPN 6,815,279 B2, hereinafter referred to as the "Yagishita" reference) discloses a similar device. Figure 1A of Yagishita discloses a semiconductor device with a buffer layer of SiGe (12) formed over a silicon substrate (10). A channel layer of silicon (13) is formed over the SiGe buffer layer (12) at a thickness of 2 nm (column 8, lines 65-67 and column 9, line 1). A gate electrode (17) is formed over the channel layer (13) with a gate insulation film (15) formed between them. A source and a drain are formed on both sides of the gate electrode (17).

8. With regard to claim 18, Yagishita (USPN 6,815,279 B2) discloses a similar fabrication method. Figures 1A, and 6A-6P of Yagishita disclose a semiconductor device and its method of fabrication such that a buffer layer of SiGe (12) formed over a silicon substrate (10). A channel layer of silicon (13) is formed over the SiGe buffer layer (12) at a thickness of 2 nm (column 8, lines 65-67 and column 9, line 1). A gate electrode (17) is formed over the channel layer (13) with a gate insulation film (15) formed between them. Figure 6E shows an implantation of a dopant impurity into the channel layer and the buffer layer using the gate electrode (24) as a mask to form first impurity diffused regions on both sides of the gate electrode (24). Figure 6F shows a sidewall insulation film (29) is formed on the sidewall of the gate electrode (24). Figure 6G shows an implantation of a dopant impurity into the channel layer and the buffer layer using the gate electrode (24) and the sidewall insulation film (29) as a mask to form second impurity diffused regions on both sides of the gate electrode (24).

***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Puchner et al. (USPN 6,544,854 B1) in view of Wilting (USPN 4,080,719).

11. In reference to claim 6, Puchner does not disclose the use of source and drain regions with nickel silicide. However Wilting (USPN 4,080,719) discloses a device in figure 16 which utilizes source and drain regions with nickel silicide (column 7, lines 61-65). Furthermore Wilting discloses that silicides provide good conductivity; which is desirable in the semiconductor art (column 1, lines 22-40 and column 7, lines 46-60). In view of Wilting, it would therefore be obvious to utilize source and drain regions with nickel silicide or cobalt silicide.

12. Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yagishita et al. (USPN 6,815,279 B2) in view of Wilting (USPN 4,080,719).

13. In reference to claims 5 and 12, Yagishita does not disclose the use of source and drain regions with nickel or cobalt silicide. However Wilting (USPN 4,080,719) discloses a device in figure 16 which utilizes source and drain regions with nickel silicide or cobalt silicide (column 7, lines 61-65). Furthermore Wilting discloses that silicides provide good conductivity; which is desirable in the semiconductor art (column 1, lines 22-40 and column 7, lines 46-60). In view of Wilting, it would therefore be obvious to utilize source and drain regions with nickel silicide or cobalt silicide.

***Allowable Subject Matter***

14. Claims 2, 3, 4, 7, 8, 10, 11, 14, 15, 16, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests or renders obvious a semiconductor device with a silicon germanium channel layer having a thickness of 2-6 nm which is formed on a silicon substrate such that the silicon germanium channel layer is only formed beneath the gate electrode.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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KVQ